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EXAMINER
NGUYEN, HIEP

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,679	MAGOON ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6,7 and 10-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7 and 10-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This is responsive to the amendment filed on 006-06-03. Applicant's arguments with respect to references of Huijsing et al. (US Pat. 4,678,947) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus the claims remained rejected under Huijsing.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The recitation "pull the electrical connection...the connectivity of the transistor circuit is not enabled by the control signal" on lines 11-16 is not disclosed in the specification. The third paragraph of page 10 of the specification only discloses the "pull up/pull down" of node (1119) to ground or to (Vcc) without disclosing the function of the transistor device (1106). It is unclear whether transistor (1106) is a P-channel or N-channel thus, the function of transistor (1106) is not defined by the polarity of the control signal.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim1 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claims 1 and 6, the recitation "...to **reduce** the effective parasitic capacitance between ... on lines 10-11 of claim 1 and "that improve the effective parasitic characteristics of the transistor circuit" on lines 14-15 of claim 6 are indefinite because they are misdescriptive. The effective parasitic capacitance between the terminals of a transistor is an **actual fixed value** of capacitance. The parasitic capacitance is an undesired by-product of the isolation process of a transistor (isolation regions, junctions). Therefore, the effective (actual) parasitic capacitance **cannot be improved or reduced**. The **effect** of the effective (actual) parasitic capacitance of the circuit can be improved or reduced by incorporating other circuit to the existing circuit.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, insofar as understood, is rejected under 35 U.S.C. 102(b) as being anticipated by Huijsing et al. (US Pat. 4,678,947).

Regarding claim 1, figure 2 of Huijsing shows a transistor circuit for implementing a switch, comprising: a first switch node (T1) configured to connect to an external circuit; a second switch node (T2) configured to connect to the external circuit; a transistor device (Q0) having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal (the base of Q0) configured to receive a control signal at node N1 that controls the electrical connectivity between the first terminal and the second terminal; a third switch node (N1) for receiving the control signal ; and an impedance circuit (A1, A2, R1, R2) connected to the third switch node (N1) and the third terminal (base) of the transistor device, the impedance circuit configured with a sufficiently high impedance to "reduce the parasitic capacitance" between the first terminal and the second terminal of the transistor device by preventing the third switch node (N1) from functioning as an alternating current ground during operation of the switch. Note that the high impedance circuit (A1, A2, R1=R2=10 Kohm) isolates node N1, during AC operation, from being connected **directly** to the

ground. As a result, the parasitic capacitances (base-emitter and base-collector) are connected in series, thus the "effective parasitic capacitance" of transistor (Q0) is reduced by that serial connection.

Claims 1 and 2, insofar as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Iliasevitch (US Pat. 6,380,644).

Regarding claims 1 and 2, figure 6 of Iliasevitch shows a transistor circuit for implementing a switch comprising: a transistor device (516) coupled to the first, second and third switch nodes, an impedance circuit (530) connected to the third switch node. The impedance circuit (530) configured with a sufficiently high impedance to "reduce the parasitic capacitance between the first terminal and the second terminal of the transistor device" by preventing the third switch node (connected to the gate of transistor 516) from functioning as an alternating current ground during operation of the switch. Note that the "high impedance" circuit (530) isolates the third node, during AC operation, from being connected **directly** to the ground. As a result, the parasitic capacitances (gate-source and gate-drain) are connected in series, thus the "effective parasitic capacitance" of transistor (516) is reduced. Transistor (516) is a MOSFET transistor.

Claims 6, 7 and 10, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US Pat. 4,752,703).

Regarding claim 6, figure 1 of Lin shows a transistor circuit for implementing a differential switch comprising: first and second switch nodes (X, Y), first and second transistors (11, 12), a third transistor (17) having a first terminal connected to the first terminal of the first transistor (11) and a second terminal connected (via 18) to the second terminal of the second transistor (12). The first, second and third transistors receive a control signal (Vin). Note that the recitation "the third transistor device configured with predetermined parasitic characteristics that improve the effective parasitic characteristics of the transistor circuit" is merely "functional language" and thus cannot be relied upon to distinguish over Lin i.e., since the reference meets all of the claim structures (and the function performed by that structure), the reference meets claim 6 under 102(b). Note that apparatus claims, to be patentable over the prior art by structure, not by the

function (result) of that structure. Note that the first, second and third transistors MOSFET transistors.

Claims 11 and 12, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Baba (US Pat. 4,574,203).

Regarding claim 11, figure 3 of Baba shows a circuit for implementing a switch comprising: a first switch node (N4), a transistor (T4n), a second switch node (connected to the source of transistor T4n), a third terminal connected to the gate of transistor (T4n) receiving a control signal from node (N2), an inverter (INV) having output connected to the second switch node for pulling the second terminal to ground providing a voltage to the second terminal. The recitation " an inverter circuit connected to the second terminal...the transistor circuit is not enabled by the control signal" on lines 9-16 is merely "functional language" and thus cannot be relied upon to distinguish over Baba i.e., since the reference meets all of the claim structures (and the function performed by that structure), the reference meets claim 6 under 102(b). Note that apparatus claims, to be patentable over the prior art by structure, not by the function (result) of that structure. Note that the first, second and third transistors MOSFET transistors.

Claims 11 and 12, insofar as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Kitamono et al. (US Pat. 6,605,963).

Regarding claim 11, figure 4 of Kitamono shows a circuit for implementing a switch comprising: a first switch node (n01), a transistor (12), a second switch node (connected to the source of transistor 12), a third terminal connected to the gate of transistor (12) receiving a control signal (IN), an inverter (14, 15) having output connected to the second switch node for pulling the second terminal to ground and providing a voltage to the second terminal. When signal (IN) is high, transistor (12) is turned on and the second node is pulled to a low level. When input signal (IN) is low, transistor (12) is turned off and the second node is pulled high. The recitation "an inverter circuit connected to the second terminal...the transistor circuit is not enabled by the control signal" on lines 9-16 is merely "functional language" and thus cannot be relied upon to distinguish over Kitamoto i.e., since the reference meets all of the claim structures (and the function performed by that structure), the reference meets claim 6 under 102(e). Note

that apparatus claims, to be patentable over the prior art by structure, not by the function (result) of that structure. Note that the first, second and third transistors MOS transistors

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al. (US Pat. 4,678,947).

Regarding claim 2, figure 2 of Huijsing includes all the limitations of the present application except for the limitation that the transistor device is a metal-oxide semiconductor FET. However, it is old and well known in the art that the MOSFET transistor and the bipolar transistor are exchangeable. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to replace the bipolar transistor (Q0) with a MOSFET transistor for saving energy and space because the MOSFET transistor is smaller than the bipolar transistor and it consumes less energy.

Response to Arguments

In the Remarks, the Applicant states that "the impedance circuit is configured with a sufficiently high impedance to **reduce** the **effective parasitic capacitance** between the first terminal and the second terminal of the transistor device...". This is not true because the effective parasitic capacitance between the terminals of a transistor is an **actual fixed value** of capacitance. The parasitic capacitance is an undesired by-product of the isolation process of a transistor (isolation regions, junctions). This " effective parasitic capacitance" cannot be changed or modified but the **effects** of the parasitic capacitance can changed by incorporating external circuits/components to the transistor. Thus claims 1 and 6 remained rejected under 112, 2nd paragraph.

The applicant also argues that Huijsing does not disclose "an impedance circuit ...configured with a sufficiently high impedance to reduce the effective parasitic capacitance ... during operation of the switch". As discussed above, the **effective parasitic capacitance** cannot be reduced. The impedance circuit of the present application is only a **blank box**. Though Huijsing does not disclose the claimed function, one skilled in the art can see that without the high impedance circuit (Fig. 2, A1, A2, R1, R2), the control terminal of transistor (Q0) will be connected directly to the ground during AC operation, thus the effect of the "effective parasitic capacitance" from the base to the emitter of Q0 is cancelled. With the impedance circuit (A1, A2, R1, R2), the control terminal (third node) of transistor (Q0) is **isolated** from the ground during AC operation and the **effect** of the "effective parasitic capacitance" between the control terminal and the ground is improved by the serial connection of the parasitic capacitances between base-emitter and base-collector. Note that terminal (TC) is **the input to the impedance circuit** (equivalent to terminal 710 of figure 7) and N1 (equivalent to terminal 712 of figure 7) is the terminal connected to the control input of transistor (Q0). During AC operation, current (IF) cannot flow backward (well known) from the outputs of A1 and A2 (node N1) to the ground. the current will flow through the high impedance elements (R1=R1=10 KOhm), thus node (N1) is not connected directly to the ground. Because node **N1 is not connected to the ground** during AC operation, the parasitic capacitance between the base/emitter and between the base/collector of transistor (Q0) are connected in series and the combined parasitic capacitance is reduced. Moreover, there is no drawing showing the detailed circuit of the blank box (708) with high impedance components, thus the performance of the impedance circuit cannot be proved.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M.. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 746-5716.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen
08-13-03

TUAN T. LAM
PRIMARY EXAMINER